THE 8085 INSTRUCTION SET

<table>
<tr><td>ACI data(8b)</td><td>Description: Add Immediate 8-bit data to the accumulator with carry.
Bytes/M-Cycles/T-States: 2/2/7
Hex Code: CE
Flags: All flags are affected based upon the result of the addition.</td></tr>
<tr><td>ADC R</td><td>Description: Add register to accumulator with carry.
Bytes/M-Cycles/T-States: 1/1/4
<table><tr><td>Hex Codes</td><td>Register</td></tr><tr><td>8F</td><td>A</td></tr><tr><td>88</td><td>B</td></tr><tr><td>89</td><td>C</td></tr><tr><td>8A</td><td>D</td></tr><tr><td>8B</td><td>E</td></tr><tr><td>8C</td><td>H</td></tr><tr><td>8D</td><td>L</td></tr></table>Flags: All flags are affected based upon the result of the addition.</td></tr>
<tr><td>ADC M</td><td>Description: Add contents of memory location pointed to by HL register pair to the accumulator with carry.
Bytes/M-Cycles/T-States: 1/2/7
Hex Codes: 8E
Flags: All flags are affected based upon the result of the addition.</td></tr>
<tr><td>ADD R</td><td>Description: Add register to accumulator.
Bytes/M-Cycles/T-States: 1/1/4
<table><tr><td>Hex Codes</td><td>Register</td></tr><tr><td>87</td><td>A</td></tr><tr><td>80</td><td>B</td></tr><tr><td>81</td><td>C</td></tr><tr><td>82</td><td>D</td></tr><tr><td>83</td><td>E</td></tr><tr><td>84</td><td>H</td></tr><tr><td>85</td><td>L</td></tr></table>Flags: All flags are affected based upon the result of the addition.</td></tr>
<tr><td>ADD M</td><td>Description: Add contents of memory location pointed to by HL to the accumulator.
Bytes/M-Cycles/T -States: 1/2/7
Hex Codes: 86
Flags: All flags are affected based upon the result of the addition.</td></tr>
<tr><td>ADI data(8b)</td><td>Description: Add the immediate 8-bit data to the accumulator.
Bytes/M-Cycles/T -States: 2/2/7
Hex Codes: C6
Flags: All flags are affected based upon the result of the addition</td></tr>
<tr><td>ANA R</td><td>Description: The contents of the accumulator and the register are logically ANDed and the result is put in the accumulator.
Bytes/M-Cycles/T-States: 1/1/4</td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>Hex Codes</td><td>Register</td></tr>
<tr><td>A 7</td><td>A</td></tr>
<tr><td>AO</td><td>B</td></tr>
<tr><td>Al</td><td>C</td></tr>
<tr><td>A2</td><td>D</td></tr>
<tr><td>A3</td><td>E</td></tr>
<tr><td>A4</td><td>H</td></tr>
<tr><td>AS</td><td>L</td></tr>
</table>
Flags: S, Z, and P arc modified based upon the result of the operation. CY is reset, and AC is set.</td></tr>
<tr><td>ANA M</td><td>Description: The contents of the accumulator and the contents of the memory location pointed to by HL are logically ANDed, and the result is put in the accumulator.
Bytes/M-Cycles/T-States: 1/2/7
Hex Codes: A6
Flags: S, Z, and P are modified based upon the result of the operation.
CY is reset, and AC is set.</td></tr>
<tr><td>ANI data(8b)</td><td>Description: The contents of the accumulator and the 8-bit data are ANDed and the result is put in the accumulator.
Bytes/M-Cycles/T-States: 2/2/7
Hex Codes: E6
Flags: S, Z, and P are modified based upon the result of the operation.
CY is reset, and AC is set.</td></tr>
<tr><td>CALL address(16b)</td><td>Description: The program sequence is transferred to the address specified by the 16-bit address. Before the program is transferred, the address of the instruction following the CALL instruction is pushed onto the stack.
Bytes/M-Cycles/T-States: 3/5/18
Hex Codes: CD
Flags: No flags are affected.</td></tr>
<tr><td>CC address(16b)</td><td>Description: The program sequence is transferred to the address specified by the 16-bit address if the CY flag is set. If CY 0, no transfer takes place. If the transfer takes place, the address of the instruction following the CC instruction is pushed onto the stack.
Bytes/M-Cycles/T-States: 3/2/9 if transfer is not taken
3/5/18 if the transfer is taken
Hex Codes: DC Flags: No flags are affected.</td></tr>
<tr><td>CNC address(16b)</td><td>Description: The program sequence is transferred to the address specified by the 16-bit address if the CY flag is not set. If CY = I, no transfer takes place. If the transfer takes place, the address of the instruction following the CNC instruction is pushed onto the stack.
Bytes/M-Cycles/T-States: 3/2/9 if transfer is not taken
3/5/18 if the transfer is taken
Hex Codes: D4
Flags: No flags are affected.</td></tr>
<tr><td>CP address (16b)</td><td>Description: The program sequence is transferred to the address specified by the 16-bit address if positive, or if the S flag = O. If S I, no transfer takes place. If the transfer takes place, the address of the instruction following the CP instruction is pushed onto the stack.</td></tr>
</table>

	Bytes/M-Cycles/T-States: 3/2/9 if transfer is not taken 3/5/18 if the transfer is taken Hex Codes: F4 Flags: No flags are affected.
CM address (16b)	Description: The program sequence is transferred to the address specified by the 16-bit address if minus, or if the S flag = 1. If S 0, no transfer takes place. If the transfer takes place, the address of the instruction following the CM instruction is pushed onto the stack. Bytes/M-Cycles/T-States: 3/2/9 if transfer is not taken 3/5/18 if the transfer is taken Hex Codes: FC Flags: No flags are affected.
CPE address (16b)	Description: The program sequence is transferred to the address specified by the 16-bit address if parity is even, or the P flag 1. If P = 0, no transfer takes place. If the transfer takes place, the address of the instruction following the CPE instruction is pushed onto the stack. Bytes/M-Cycles/T-States: 3/2/9 if transfer is not taken 3/5/18 if the transfer is taken Hex Codes: EC Flags: No flags affected.
CPO address (16b)	Description: The program sequence is transferred to the address specified by the 16-bit address if parity is odd, or if the P flag O. If P = 1, no transfer takes place. If the transfer takes place, the address of the instruction following the CPO instruction is pushed onto the stack. Bytes/M-Cycles/T-States: 3/2/9 if transfer is not taken 3/5/18 if the transfer is taken Hex Codes: E4 Flags: No flags are affected.
CZ address (16b)	Description: The program sequence is transferred to the address specified by the 16-bit address if zero, or if the Z flag 1. If Z = 0, no transfer takes place. If the transfer takes place, the address of the instruction following the CZ instruction is pushed onto the stack. Bytes/M-Cycles/T-States: 3/2/9 if transfer is not taken 3/5/18 if the transfer is taken Hex Codes: CC Flags: No flags are affected.
CNZ address(16b)	Description: The program sequence is transferred to the address specified by the 16-bit address if not zero, or if the Z flag O. If Z = 1, no transfer takes place. If the transfer takes place, the address of the instruction following the CNZ instruction is pushed onto the stack. Bytes/M-Cycles/T-States: 3/2/9 if transfer is not taken 3/5/18 if the transfer is taken Hex Codes: C4 Flags: No flags arc affected.
CMA	Description: The contents of the accumulator are con1.plemented. Bytes/M-Cycles/T-States: 1/1/4 Hex Codes: 2F Flags: No flags arc affected.
CMC	Description: The carry flag is complemented. Bytes/M-Cycles/T-States: 1/1/4 Hex Codes: 3F Flags: The CY flag is complemented. No other flags are affected.
CMP R	Description: The contents of the register are compared to the contents of the accumulator. Both contents are unaffected, and the following flags are used to show the results of the compare: If A < R CY 1 and Z = 0 If A R CY = 0 and Z = 1 If A > R

<table>
<tr><td></td><td>CY = 0 and Z 0 Bytes/M-Cycles/T-States: 1/1/4
<table>
<tr><td>Hex Codes</td><td>Registers</td></tr>
<tr><td>BF</td><td>A</td></tr>
<tr><td>B8</td><td>B</td></tr>
<tr><td>B9</td><td>C</td></tr>
<tr><td>BA</td><td>D</td></tr>
<tr><td>BB</td><td>E</td></tr>
<tr><td>BC</td><td>H</td></tr>
<tr><td>BD</td><td>L</td></tr>
</table>
Flags: S, P, and AC are also affected based upon the results of the operation, besides Z and CY.</td></tr>
<tr><td>CMP M</td><td>Description: The contents of the memory location pointed to by HL are compared to the contents of the accumulator. Both contents are unaffected, and the following flags are used to show the results of the Compare:
If A < R CY = 1 and Z = 0
If A = R CY = 0 and Z = 1
If A > R CY = 0 and Z = 0
Bytes/M-Cycles/T-States: 1/2/7
Hex Codes: BE Flags: S, P, and AC are also affected based upon the results of the operation, besides Z and CY.</td></tr>
<tr><td>CPI data(8b)</td><td>Description: The 8-bit data is compared with the contents of the accumulator. The contents of the accumulator are unaffected. The following flags are used to show the results of the compare:
If A < R CY= 1 and Z = 0
If A = R CY = 0 and Z = 1
If A > R CY = 0 and Z = 0
Bytes/M-Cycles/T-States: 2/2/7
Hex Codes: FE
Flags: S, P, and AC are also affected based upon the results of the operation, besides Z and CY.</td></tr>
<tr><td>DAA</td><td>Description: The contents of the accumulator arc converted from a binary value to two 4-bit Binary Coded Decimal (BCD) digits.
Bytes/M-Cycles/T-States: 1/1/4
Hex Codes: 27
Flags: S, Z, AC, P, and CY flags are affected based upon the results of the operation</td></tr>
<tr><td>DAD Rp</td><td>Description: The contents of the register pair (Rp) are added to the contents of the register pair HL. The source register pair is unchanged, and the results are stored in HL. Bytes/M-Cycles/T-States: 1/3/10
<table>
<tr><td>Hex Codes:</td><td>Register Pair</td></tr>
<tr><td>09</td><td>BC</td></tr>
<tr><td>19</td><td>DE</td></tr>
<tr><td>29</td><td>HL</td></tr>
<tr><td>39</td><td>SP</td></tr>
</table>
Flags: If the result is larger than 16 bits, the CY flag is set, otherwise no flags are affected.</td></tr>
<tr><td>DCR R</td><td>Description: The contents of the register are decremented by one. The result is stored in the register. Bytes/M-Cycles/T-States: 1/1/4</td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>Hex Codes:</td><td>Register</td></tr>
<tr><td>3D</td><td>A</td></tr>
<tr><td>05</td><td>B</td></tr>
<tr><td>0D</td><td>C</td></tr>
<tr><td>15</td><td>D</td></tr>
<tr><td>ID</td><td>E</td></tr>
<tr><td>25</td><td>H</td></tr>
<tr><td>2D</td><td>L</td></tr>
</table>
Flags: S, AC, Z, and P are affected by the results of the operation. The CY flag is not affected.
</td></tr>
<tr><td>DCR M</td><td>Description: The contents of the memory location pointed to by HL are decremented by one, and the results are stored in the memory location.
Bytes/M-Cycles/T-States: 1/3/10
Hex Code: 35
Flags: S, AC, Z, and P arc affected by the results of the operation. The CY flag is not affected.</td></tr>
<tr><td>DCX Rp</td><td>Description: The contents of the register pair are decremented by 1. The result is stored in the register pair. The register pair is treated as a 16-bit number. Bytes/M-Cycles/T -States: 1/1/6
<table>
<tr><td>Hex Codes:</td><td>Register Pair</td></tr>
<tr><td>0B</td><td>BC</td></tr>
<tr><td>1B</td><td>DE</td></tr>
<tr><td>2B</td><td>HL</td></tr>
<tr><td>3B</td><td>SP</td></tr>
</table>
Flags: No flags are affected.</td></tr>
<tr><td>DI</td><td>Description: The Interrupt Enable flip-flop is reset, and all of the interrupts except the TRAP interrupt are disabled. Bytes/M-Cycles/T-States: 1/1/4 Hex Codes: F3 Flags: No flags are affected.</td></tr>
<tr><td>EI</td><td>Description: The interrupt Enable flip-flop is set and all interrupts are enabled.
Bytes/M-Cycles/T-States: 1/1/4
Hex Codes: FB
Flags: No flags are affected.</td></tr>
<tr><td>HLT</td><td>Description: The MPU finishes executing the current instruction and halts any further execution. The MPU enters the Halt Acknowledge machine cycle, and Wait states are inserted in every clock period. It requires an interrupt or a reset to get the MPU out of the Halt state.
Bytes/M-Cycles/T-States: One / two or more / five or more
Hex Codes: 76
Flags: No flags are affected.</td></tr>
<tr><td>IN port address(8b)</td><td>Description: The contents of the input port designated are read and loaded into the accumulator.
Bytes/M-Cycles/T-States: 2/3/10
Hex Codes: DB
Flags: No flags are affected.</td></tr>
<tr><td>INR R</td><td>Description: The contents of the register are incremented by one and stored in the register.
Bytes/M-Cycles/T-States: 1/1/4</td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>Hex Codes</td><td>Register</td></tr>
<tr><td>3C</td><td>A</td></tr>
<tr><td>04</td><td>13</td></tr>
<tr><td>OC</td><td>C</td></tr>
<tr><td>14</td><td>D</td></tr>
<tr><td>1C</td><td>E</td></tr>
<tr><td>24</td><td>H</td></tr>
<tr><td>2C</td><td>L</td></tr>
</table>
Flags: S, Z, P, AC arc affected by the results of the operation. CY is not modified.</td></tr>
<tr><td>INR M</td><td>Description: The contents of the memory location pointed to by HL are incremented by one and the result is put in the memory location.
Bytes/M-Cycles/T-States: 1/3/10
Hex Codes: 34
Flags: S, Z, P, and AC are affected by the results of the operation. CY is not modified.</td></tr>
<tr><td>INX Rp</td><td>Description: The contents of the register pair are increnlented by 1 and stored in the register pair. The instruction views the two registers as a 16-bit number. Bytes/M-Cycles/T-States: 1/1/6
<table>
<tr><td>Hex Codes:</td><td>Register Pair</td></tr>
<tr><td>03</td><td>BC</td></tr>
<tr><td>13</td><td>DE</td></tr>
<tr><td>23</td><td>HL</td></tr>
<tr><td>33</td><td>SP</td></tr>
</table>
Flags: No flags are affected.</td></tr>
<tr><td>JMP address(16b)</td><td>Description: The program execution is transferred to the memory address specified.
Bytes/M-Cycles/T-States: 3/3/10
Hex Codes: C3
Flags: No flags are affected.</td></tr>
<tr><td>JC address(16b)</td><td>Description: Program execution is transferred to the memory address specified if the carry flag is set, or CY = 1. If CY =, 0, no transfer takes place.
Bytes/M-Cycles/T-States: 3/2/7 if condition is not true
3/3/10 if condition is true
Hex Codes: DA
Flags: No flags arc affected.</td></tr>
<tr><td>JNC address(16b)</td><td>Description: Program execution is transferred to the memory address specified if the carry flag is not set, or CY = 0. If CY = 1, no transfer takes place.
Bytes/M-Cycles/T-States: 3/2/7 if condition is not true
3/3/10 if condition is true
Hex Codes: D2
Flags: No flags arc affected.</td></tr>
<tr><td>JP address (16b)</td><td>Description: Program execution is transferred to the memory address specified if positive, or S = 0. If S = 1, no transfer takes place.
Bytes/M-Cycles/T-States: 3/2/7 if condition is not true
3/3/10 if condition is true
Hex Codes: F2
Flags: No flags are affected.</td></tr>
<tr><td>JM address (16b)</td><td>Description: Program execution is transferred to the memory address specified if minus, or S 1. If S = 0, no transfer takes place.</td></tr>
</table>

<table>
<tr><td></td><td>Bytes/M-Cycles/T-States: 3/2/7 if condition is not true
3/3/10 if condition is true
Hex Codes: FA
Flags: No flags are affected.</td></tr>
<tr><td>JPE address(16b)</td><td>Description: Program execution is transferred to the memory address specified if parity is even, or P = 1. If P 0, no transfer takes place.
Bytes/M-Cycles/T-States: 3/2/7 if condition is not true
3/3/10 if condition is true
Hex Codes: EA
Flags: No flags are affected.</td></tr>
<tr><td>JPO address(16b)</td><td>Description: Program execution is transferred to the memory address specified if parity is odd, or P O. If P I, no transfer takes place.
Bytes/M-Cycles/T-States: 3/2/7 if condition is not true
3/3/10 if condition is true
Hex Codes: E2
Flags: No flags are affected.</td></tr>
<tr><td>JZ address (16b)</td><td>Description: Program execution is transferred to the memory address specified if zero, or Z = 1. If Z = 0, no transfer takes place.
Bytes/M-Cycles/T-States: 3/2/7 if condition is not true
3/3/10 if condition is true
Hex Codes: CA
Flags: No flags are affected.</td></tr>
<tr><td>JNZ address(16b)</td><td>Description: Program execution is transferred to the memory address specified if not zero, or Z = 0. If Z = 1, no transfer takes place.
Bytes/M-Cycles/T-States: 3/2/7 if condition is not true
3/3/10 if condition is true
Hex Codes: C2
Flags: No flags are affected.</td></tr>
<tr><td>LDA address(16b)</td><td>Description: The contents of the memory location specified are transferred to the accumulator.
Bytes/M-Cycles/T-States: 3/4/13
Hex Codes: 3A
Flags: No flags are affected.</td></tr>
<tr><td>LDAX Rp</td><td>Description: The contents of the memory location pointed to by the register pair are loaded into the accumulator.
Bytes/M-Cycles/T-States: 1/2/7
<table>
<tr><td>Hex Codes:</td><td>Register Pairs</td></tr>
<tr><td>0A</td><td>BC</td></tr>
<tr><td>1A</td><td>DE</td></tr>
</table>
Flags: No flags are affected.</td></tr>
<tr><td>LHLD address(16b)</td><td>Description: The contents of the memory location specified are
loaded into register L and the contents of the next memory location are loaded into register H.
Bytes/M-Cycles/T-States: 3/5/16
Hex Codes: 2A
Flags: No flags are affected</td></tr>
<tr><td>LXI Rp, data(16b)</td><td>Description: The 16-bit data is loaded into the register pair. Bytes/M-Cycles/T-States: 3/3/10</td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><th>Hex Codes</th><th>Register Pair</th></tr>
<tr><td>01</td><td>BC</td></tr>
<tr><td>11</td><td>DE</td></tr>
<tr><td>21</td><td>HL</td></tr>
<tr><td>31</td><td>SP</td></tr>
</table>
Flags: No flags are affected.
</td></tr>
<tr><td>MOV Rd, Rs</td><td>Description: The contents of the source register Rs are transferred into the destination register Rd.
Bytes/M-Cycles/T-States: 1/1/4
Hex Codes:
<table>
<tr><td rowspan="2">Destination Register</td><td colspan="8">Source Register</td></tr>
<tr><td></td><td>A</td><td>B</td><td>C</td><td>D</td><td>E</td><td>H</td><td>L</td></tr>
<tr><td>A</td><td>7F</td><td>78</td><td>79</td><td>7A</td><td>7B</td><td>7C</td><td>7D</td></tr>
<tr><td>B</td><td>47</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td></tr>
<tr><td>C</td><td>41</td><td>48</td><td>49</td><td>4A</td><td>4B</td><td>4C</td><td>4D</td></tr>
<tr><td>D</td><td>57</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td></tr>
<tr><td>E</td><td>SF</td><td>58</td><td>59</td><td>SA</td><td>5B</td><td>5C</td><td>5D</td></tr>
<tr><td>H</td><td>67</td><td>60</td><td>61</td><td>62</td><td>63</td><td>64</td><td>65</td></tr>
<tr><td>L</td><td>6F</td><td>68</td><td>69</td><td>6A</td><td>6B</td><td>6C</td><td>6D</td></tr>
</table>
Flags: No flags arc affected.</td></tr>
<tr><td>MOVM,Rs</td><td>Description: The contents of the source register Rs are transferred to the memory location pointed to by HL. Bytes/M-Cycles/T-States: 1/2/7
<table>
<tr><th>Hex Codes:</th><th>Source Register</th></tr>
<tr><td>77</td><td>A</td></tr>
<tr><td>70</td><td>B</td></tr>
<tr><td>71</td><td>C</td></tr>
<tr><td>72</td><td>D</td></tr>
<tr><td>73</td><td>E</td></tr>
<tr><td>74</td><td>H</td></tr>
<tr><td>75</td><td>L</td></tr>
</table>
Flags: No flags are affected.</td></tr>
<tr><td>MOV Rd, M</td><td>Description: The contents of the memory location pointed to by HL are transferred to the destination register.
Bytes/M-Cycles/T-States: 1/2/7
<table>
<tr><th>Hex Codes</th><th>Destination Register</th></tr>
<tr><td>7E</td><td>A</td></tr>
<tr><td>46</td><td>B</td></tr>
<tr><td>4E</td><td>C</td></tr>
<tr><td>56</td><td>D</td></tr>
<tr><td>5E</td><td>E</td></tr>
<tr><td>66</td><td>H</td></tr>
<tr><td>6E</td><td>L</td></tr>
</table>
Flags: No flags are affected.</td></tr>
<tr><td>MVI R, data(8b)</td><td>Description: The 8 bits of data are stored in the register.
Bytes/M-Cyc1es/T-States: 2/2/7</td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>Hex Codes:</td><td>Register</td></tr>
<tr><td>3E</td><td>A</td></tr>
<tr><td>06</td><td>B</td></tr>
<tr><td>OE</td><td>C</td></tr>
<tr><td>16</td><td>D</td></tr>
<tr><td>IE</td><td>E</td></tr>
<tr><td>26</td><td>H</td></tr>
<tr><td>2E</td><td>L</td></tr>
</table>
Flags: No flags are affected.</td></tr>
<tr><td>MVI M, data(8b)</td><td>Description: The 8 bits of data are stored in the memory location pointed to by HL.
Bytes/M-Cyc1es/T-States: 2/3/10
Hex Codes: 36
Flags: No flags are affected.</td></tr>
<tr><td>NOP</td><td>Description: No operation is performed. The instruction is fetched and decoded, but no operation is executed.
Bytes/M-Cyc1es/T -States: 1/1/4
Hex Codes: 00
Flags: No flags are affected.</td></tr>
<tr><td>ORA R</td><td>Description: The contents of the accumulator are logically OR'd with the contents of the register. The result is stored in the accumulator.
Bytes/M-Cyc1es/T -States: 1/1/4
<table>
<tr><td>Hex Codes:</td><td>Register</td></tr>
<tr><td>B7</td><td>A</td></tr>
<tr><td>B0</td><td>B</td></tr>
<tr><td>B1</td><td>C</td></tr>
<tr><td>B2</td><td>D</td></tr>
<tr><td>B3</td><td>E</td></tr>
<tr><td>B4</td><td>H</td></tr>
<tr><td>B5</td><td>L</td></tr>
</table>
Flags: Z, S, and P are affected based upon the operation. AC and CY are reset.</td></tr>
<tr><td>ORAM</td><td>Description: The contents of the accumulator are logically OR'd with the contents of the memory location pointed to by HL.
Bytes/M-Cycles/T-States: 1/2/7
Hex Codes: B6
Flags: Z, S, and P are affected based upon the operation. AC and CY are reset.</td></tr>
<tr><td>ORI data(8b)</td><td>Description: The contents of the accumulator are logically OR'd with the 8 bits of data. The result is stored in the accumulator.
Bytes/M-Cycles/T -States: 2/2/7
Hex Codes: F6
Flags: Z, S, and P are affected based upon the operation. AC and CY are reset.</td></tr>
<tr><td>OUT port address(8b)</td><td>Description: The contents of the accumulator are copied out to the output port specified.
Bytes/M-Cycles/T-States: 2/3/10
Hex Codes: D3
Flags: No flags are affected.</td></tr>
<tr><td>PCHL</td><td>Description: The contents of registers Hand L are copied into the program counter. H is the high-order bits and L is the low-order bits.
Bytes/M-Cycles/T-States: 1/1/6
Hex Codes: E9
Flags: No flags are affected.</td></tr>
</table>

<table>
<tr><td>POP Rp</td><td>Description: The contents of the memory location (stack) pointed to by the stack pointer are copied to the low-order register of the register pair. (C, E, L, and flags.) The stack pointer is then incremented and
the contents of that memory location being pointed to are copied to the high-order register of the register pair.
Bytes/M-Cycles/T-States: 1/3/10 pair.
Bytes/M-Cycles/T-States: 1/3/10
<table><tr><td>Hex Codes:</td><td>Register</td></tr><tr><td>C1</td><td>BC</td></tr><tr><td>D1</td><td>DE</td></tr><tr><td>E1</td><td>HL</td></tr><tr><td>F1</td><td>PSW</td></tr></table>Flags: No flags are affected.</td></tr>
<tr><td>PUSH Rp</td><td>Description: The contents of the register pair are copied into the stack. The high-order register (B, D, H, A) is put on the stack first, then the contents of the low-order register (C, E, L, flags) are put onto the stack.
Bytes/M-Cycles/T-States: 1/3/12
<table><tr><td>Hex Codes:</td><td>Register Pair</td></tr><tr><td>C5</td><td>B</td></tr><tr><td>D5</td><td>D</td></tr><tr><td>E5</td><td>H</td></tr><tr><td>F5</td><td>PSW</td></tr></table>Flags: No flags are affected.</td></tr>
<tr><td>RAL</td><td>Description: The contents of the accumulator are rotated left by one position through the carry flag.
Bytes/M-Cycles/T-States: 1/1/4
Hex Codes: 17
Flags: CY is modified according to bit D7. S, Z, P, and AC are not affected.</td></tr>
<tr><td>RAR</td><td>Description: The contents of the accumulator are rotated right by one position through the carry flag.
Bytes/M-Cycles/T-States: 1/1/4
Hex Codes: IF
Flags: CY is modified according to bit DO. S, Z, P, and AC are not affected.</td></tr>
<tr><td>RLC</td><td>Description: The contents of the accumulator are rotated left one position. Bit D7 is placed in both DO and CY.
Bytes/M-Cycles/T-States: 1/1/4
Hex Codes: 07
Flags: CY is modified according to bit D7. S, Z, P, and AC are not affected.</td></tr>
<tr><td>RRC</td><td>Description: The contents of the accumulator are rotated right by 1 bit. Bit DO is placed in both D7 and CY at the same time.
Bytes/M-Cycles/T-States: 1/1/4
Hex Codes: OF
Flags: CY is modified according to bit DO. S, Z, P, and AC are not affected.</td></tr>
<tr><td>RET</td><td>Description: The program sequence is transferred from the subroutine to the calling program. The two bytes from the top of the stack are copied into the Program Counter and this is the address that program execution begins.
Bytes/M-Cycles/T-States: 1/3/10
Hex Codes: C9</td></tr>
</table>

	Flags: No flags are affected.
RC	Description: The program sequence is transferred from the subroutine to the calling program if the carry flag is set, or CY = 1. If CY = 0, no transfer takes place. Bytes/M-Cycles/T -States: 1/1/6 if condition is not true 1/3/12 if condition is true Hex Codes: D8 Flags: No flags are affected.
RNC	Description: The program sequence is transferred from the subroutine to the calling program if the carry flag is not set, or CY = O. If CY = I, no transfer takes place. Bytes/M-Cycles/T-States: 1/1/6 if condition is not true 1/3/12 if condition is true Hex Codes: D0 Flags: No flags are affected.
RP	Description: the program sequence is transferred from the subroutine to the calling program if positive, or S O. If S I, no transfer takes place. Bytes/M-Cycles/T-States: 1/1/6 if condition is not true 1/3/12 if condition is true Hex Codes:F0 Flags: No flags are affected.
RM	Description: The program sequence is transferred from the subroutine to the calling program if minus, or S = 1. If S = 0, no transfer takes place. Bytes/M-Cycles/T-States: 1/1/6 if condition is not true 1/3/12 if condition is true Hex Codes: F8 Flags: No flags arc affected.
RPE	Description: The program sequence is transferred from the subroutine to the calling program if the parity is even, or P = 1. If P = 0, no transfer takes place. Bytes/M-Cycles/T-States: 1/1/6 if condition is not true 1/3/12 if condition is true Hex Codes: E8 Flags: No flags are affected.
RPO	Description: The program sequence is transferred from the subroutine to the calling program if the parity is odd, or P = O. If P = I, no transfer takes place. Bytes/M-Cycles/T-States: 1/1/6 if condition is not true 1/3/12 if condition is true Hex Codes: EO Flags: No flags arc affected
RZ	Description: The program sequence is transferred from the subroutine to the calling program if zero, or Z = 1. If Z 0, no transfer takes place. Bytes/M-Cycles/T-States: 1/1/6 if condition is not true 1/3/12 if condition is true Hex Codes: C8 Flags: No flags are affected.
RNZ	Description: The program sequence is transferred from the subroutine to the calling program if not zero, or Z = 0. If Z = 1, no transfer takes place. Bytes/M -Cycles/T -States: 1/1/6 if condition is not true 1/3/12 if condition is true

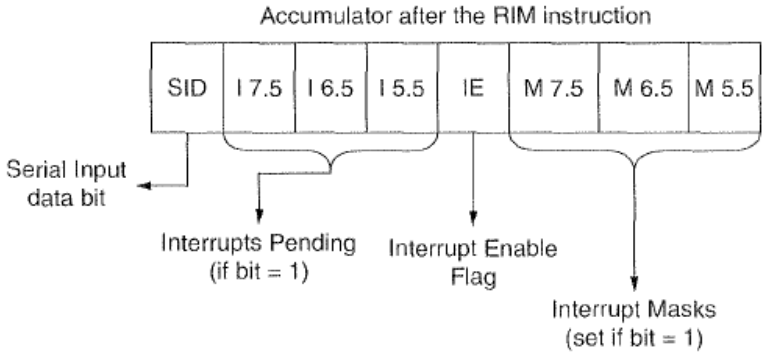
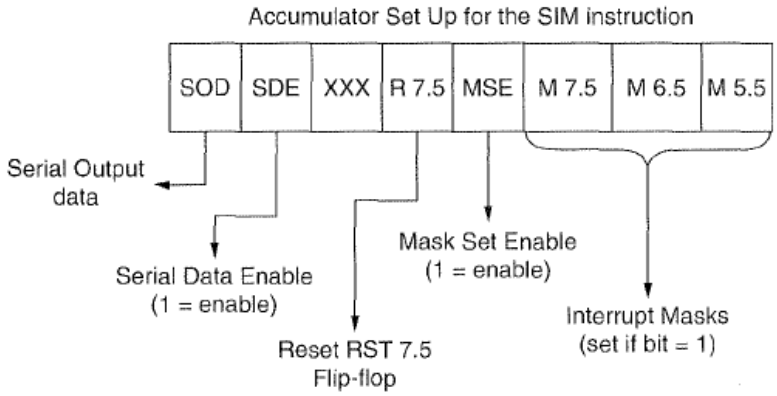
<table>
<tr><td></td><td>Hex Codes: C0
Flags: No flags are affected.</td></tr>
<tr><td>RIM</td><td>Description: This instruction is used to both read in the status of interrupts 7.5, 6.5, and 5.5, as well as to read in the serial input data bit. An 8-bit word is read in and stored in the accumulator. The layout of that word is shown in Figure AI-I.
Bytes/M-Cycles/T-States: 1/1/4
 

Figure A1-1 ■ The RIM instruction layout in the accumulator
Hex Codes: 20
Flags: No flags are affected.</td></tr>
<tr><td>RST n
(where
n=0-7)</td><td>Description: This instruction operates like a call instruction that goes to one of eight predetermined memory locations on page 0. Each instruction (RST 0-RST 7) goes to a specific address listed next.
<table>
<tr><td>Instruction</td><td>Restart Address</td></tr>
<tr><td>RST0</td><td>0000</td></tr>
<tr><td>RST1</td><td>0008</td></tr>
<tr><td>RST2</td><td>0010</td></tr>
<tr><td>RST3</td><td>0018</td></tr>
<tr><td>RST4</td><td>0020</td></tr>
<tr><td>RST5</td><td>0028</td></tr>
<tr><td>RST6</td><td>0030</td></tr>
<tr><td>RST7</td><td>0038</td></tr>
</table>
Bytes/M-Cycles/T-States: 1/3/12
<table>
<tr><td>Hex Codes:</td><td>Restart Address</td></tr>
<tr><td>C7</td><td>RST0</td></tr>
<tr><td>CF</td><td>RST1</td></tr>
<tr><td>D7</td><td>RST2</td></tr>
</table></td></tr>
</table>

<table>
<tr><td></td><td>
<table>
<tr><td>DF</td><td>RST3</td></tr>
<tr><td>E7</td><td>RST4</td></tr>
<tr><td>EF</td><td>RST5</td></tr>
<tr><td>F7</td><td>RST6</td></tr>
<tr><td>FF</td><td>RST7</td></tr>
</table>
Flags: No flags are accepted.
</td></tr>
<tr><td>SBB R</td><td>Description: The contents of the register and the borrow flag are subtracted from the contents of the accumulator and the results are stored in the accumulator.
Bytes/M-Cycles/T-States: 1/1/4
<table>
<tr><td>Hex Codes:</td><td>Register</td></tr>
<tr><td>9F</td><td>A</td></tr>
<tr><td>98</td><td>B</td></tr>
<tr><td>99</td><td>C</td></tr>
<tr><td>9A</td><td>D</td></tr>
<tr><td>9B</td><td>E</td></tr>
<tr><td>9C</td><td>H</td></tr>
<tr><td>9D</td><td>L</td></tr>
</table>
Flags: All flags are affected based upon the results of the operation.</td></tr>
<tr><td>SBB M</td><td>Description: The contents of the memory location pointed to by HL and the borrow flag are subtracted from the contents of the accumulator. The results are then stored in the accumulator.
Bytes/M-Cycles/T-States: 1/2/7
Hex Codes: 9E Flags: All flags are affected based upon the results of the operation.</td></tr>
<tr><td>SBI data(8b)</td><td>Description: The 8 bit data and borrow flags are subtracted from the accumulator and the results are stored in the accumulator .
Bytes/M-Cycles/T-States: 2/2/7
Hex Codes: DE
Flags: All flags are affected based upon the result of the operation.</td></tr>
<tr><td>SHLD address[16b]</td><td>Description :The contents of register L are stored at the memory location specified and the contents of register H are stored at the next memory location by incrementing the operand by 1.
Bytes/M-Cycles/T-States: 3/5/16
Hex Codes: 22
Flags: No flags are affected.</td></tr>
<tr><td>SIM</td><td>Description: This is an instruction that is used to set the interrupt masks as well as set the serial output data bit. The accumulator is laid out as shown in Figure Al-2 Accumulator Set Up for the SIM instruction</td></tr>
</table>

	 **Figure A1-2** ■ The SIM instruction accumulator layout
SPHL	Description: The contents of registers Hand L are loaded into the Stack Pointer. H has the high-order part of the address, while L has the low-order portion. Bytes/M-Cycles/T-States: 1/1/6 Hex Codes: F9 Flags: No flags are affected.
STA address [16b]	Description: The contents of the accumulator are stored at the memory location specified. Bytes/M-Cycles/T-States: 3/4/13 Hex Codes: 32 Flags: No flags are affected.
STAX Rp (only BC or DE)	Description: The contents of the accumulator are stored at the memory location pointed to by the register pair. The contents of the accumulator are not affected. Bytes/M-Cycles/T·States: 1/2/7 Register Pair Hex Codes: 02 BC 12 DE Flags: No flags are affected.
STC	Description: The carry flag, CY, is set to 1. Bytes/M-Cycles/T-States: 1/1/4 Hex Codes: 37 Flags: Only the CY flag is affected.
SUBR	Description: The contents of the register are subtracted from the accumulator and the result is stored in the accumulator. Bytes/M-Cycles/T-States: 1/1/4 Register Hex Codes: 97 A 90 B 91 C 92 D 93 E 94 H 95 L
SUBM	Description: The contents of the memory location pointed to by HL are subtracted from the accumulator and the result is stored in the accumulator. Bytes/M-Cycles/T-States: 1/2/7

	Hex Codes: 96 Flags: All flags are affected by the result of the operation.
SUI data(8b)	Description: The 8-bit data is subtracted from the contents of the accumulator. The result is stored in the accumulator. Bytes/M-Cycles/T -States: 2/2/7 Hex Codes: D6 Flags: All flags are affected by the result of the operation.
XCHG	Description: The contents of register H and register D are exchanged, and the contents of register L and register E are exchanged. Bytes/M-Cycles/T-States: 1/1/4 Hex Codes: EB Flags: No flags arc affected.
XRAR	Description: The contents of the register are Exclusive OR'd with the contents of the accumulator. The results are then stored in the accumulator. Bytes/M-Cycles/T -States: 1/1/4 Register Hex Codes: AF A A8 B A9 C AA D AB E AC H AD L Flags: Z, 5, and P are affected based upon the operation. CY and AC are reset.
XRAM	Description: The contents of the memory location pointed to by HL are Exclusive OR'd with the contents of the accumulator. The results are stored in the accumulator. Bytes/M-Cycles/T -States: 1/2/7 Hex Codes: AE Flags: Z, 5, and P are affected based upon the operation. CY and AC are reset.
XRI data(8b)	Description: The 8 bits of data arc Exclusive OR'd with the contents of the accumulator. The results are then stored in the accumulator. Bytes/M-Cycles/T-States: 2/2/7 Hex Codes: EE Flags: Z, 5, and P arc affected based upon the operation. CY and AC are reset.
XTHL	Description: The contents of the L register are exchanged with the stack location pointed to by the stack pointer. The contents of the H register arc exchanged with the stack location pointed to by the stack pointer +1. The stack pointer remains unchanged. Bytes/M-Cycles/T-States: 1/5/16 Hex Codes: E3 Flags: No flags are affected.

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